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ANALOG TO DIGITAL CONVERTER UTILIZING RESOLUTION ENHANCEMENT

by

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ANALOG TO DIGITAL CONVERTER
UTILIZING RESOLUTION ENHANCEMENT

STATEMENT AS TO RIGHTS TO INVENTIONS MADE UNDER
FEDERALLY SPONSORED RESEARCH AND DEVELOPMENT

BACKGROUND OF THE INVENTION

10   **1.   Field of the Invention**

The invention relates to analog to digital converters and more specifically, to an analog to digital converter providing resolution enhancement utilizing a reduced span analog to digital converter.

2.   Description of the Related Art

15   General Background

Analog to digital converters are circuit blocks which convert a span of analog voltages to digital numbers. It is customary to characterize this digital number, and consequently, the converter's resolution by the number of bits it contains.

As a first example, if the digital output is composed of eight bits, the output

20   number can take on any of $2^8 = 256$ values. The analog input span's dynamic range is thus considered to be divided into 256 discrete quanta for an eight bit converter.

As a second example, if the output is composed of 10 bits, the output number can take on any of $2^{10} = 1024$ values. The analog input span's dynamic range is thus considered to be divided into 1024 discrete quanta for a 10 bit converter.

The mathematical reason for this is that a single bit represents <u>two</u> states, customarily referred to as a "1" and a "0". If there are eight bits, the total number of combinations of "1s" and "0s" is 2^8.

Input signals exceeding the converter's input span (also referred to as its dynamic range) typically result in undefined behavior.

The complexity of an analog to digital converter is strongly related to the number of bits it can provide: In general, the more bits which are required, the more complex the converter is. Converter complexity adversely influences its cost and development schedule. From a cost and schedule perspective, it is desirable to develop a converter having only a small number of bits. Unfortunately, many applications require high resolution to meet overall system requirements. This may force a resultant complexity onto the analog to digital converter.

The hereinafter described invention offers a means of compromise between converter resolution (the number of bits) and converter complexity.

3. Statement of the Problem

Analog to digital converters having relatively high resolution are often needed to satisfy a system's requirements. Some circumstances allow the converter to be replaced by a special input preamplifier and a simpler converter, one providing few bits. This

lowers overall circuit design complexity. The reduction in number of converter bits is compensated for by offset voltages applied to a special input amplifier.

Alternate and Prior Solutions to the Problem

High resolution conversion

5   The straightforward solution to the problem of digitizing at high resolution is to use a high resolution analog to digital converter. This technique is illustrated in Fig. 1 of the drawing.

Figure 1 shows as an example the transfer function of a system whose analog to digital converter's input span matches the system's full input signal range. To achieve

10   this match, the input signal was appropriately amplified as shown. In this example, the signal source input is plotted along the horizontal axis and extends between values of -0.01 and +0.1. This input signal is amplified by a conventional analog circuit to provide an output signal extending between values of -4 and +4. This amplified output signal is applied to the analog to digital converter's input. The converter's input span is

15   typically designed to coincide with the full range of the amplified signal thereby taking advantage of the analog to digital converter's entire dynamic range. The converter's span as shown in the figure extends across the entire vertical axis of the figure.

If the system requirements state, for example, the input signal must be resolved to one part in 10,000, then a converter having at least 14 bits is required. Thirteen bits

20   is insufficient as the following computations illustrate:

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$2^{13} = 8192$ The number of values a 13 bit converter can resolve.

$2^{14} = 16,384$ The number of values a 14 bit converter can resolve.

Since the required resolution is greater than that offered by a 13 bit converter, an additional 14th bit is required. This greatly complicates the converter's design.

5   **Low-Resolution, Over-Sampled Converters ("Sigma-Delta" Converters)**

A second means of utilizing low resolution converters for precision measurements is to sample the input signal at a high rate with the low-resolution converter. The digital output of the converter is reconstructed into an analog signal, also at the high rate. The reconstructed analog signal is compared with the original

10   analog signal using a precision comparator circuit. If the reconstructed signal is higher than the input, the digital output of the converter is mathematically reduced and the reduced value converted to an analog value which is again compared to the input signal. This process continues until the reconstructed signal is smaller than the input The reconstructed signal is then mathematically incremented until it is again larger than the

15   input.

This has the effect of causing the reconstructed analog voltage to lock onto the input voltage in a servo-loop fashion. The mathematically determined values are applied to a digital filter whose output, at a much slower rate, is a precision digital representation of the input signal.

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These types of converters are referred to as "sigma-delta" converters and can

provide high performance. For example, an analog to digital converter consisting of a

single bit can be used to provide a conversion whose resolution can exceed 20 bits.

A disadvantage of these converters is they cannot easily track rapidly changing

5   input signals. It is easy for their servo-lock on the input signal to become broken if the

slew rate of the input signal exceeds a fixed amount.

Patent Literature

U.S. Patent 4,183,016, Sawagata, "Parallel Analog-To-Digital Converter With
Increased Resolution"

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This patent utilizes an offset reference voltage to reduce the level of the input

signal. However, this patent reduces the input signal by only a single, least significant

bit, which is then added on to the converted signal. In contrast, the present AD

converter system separately converts a reference voltage, comprised of potentially more

15   than a least significant bit. This voltage is then subtracted from the input voltage, which

is then converted. The converted reference voltage is then added to the converted

reduced input voltage. The present invention allows for a greater improved resolution,

for input signals which have a large DC level imposed on a small AC signal.

U.S. Patent No. 5,250,948, Berstein et al., "High Level Resolution
20   Enhancement for Dual-Range A/D Conversion"

This patent discloses a dual range A/D in which there are two possible signal

paths. If the input signal is small, then the first path, which contains an input

amplification, is used. If the input signal is large, the second path, which contains unity

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gain, is used. In contrast, the present AD converter system utilizes a single input path in which the input is reduced by an offset voltage to eliminate any DC component of the signal. The preconverted offset is then added to the signal conversion to provide the conversion of the full input signal.

5   U.S. Patent No. 5,608,399, Coleman, Jr., "Resolution Enhancer Circuit for Analog to Digital Conversion"

This patent provides conversion to a wide ranging analog input signal. If the signal exceeds the limit of the A/D, then the input is scaled down. If the input is much

10   less than the range of the A/D, then the input is scaled up. The difference between the prescaled and scaled signal is separately input to the A/D to provide the final converted output. In contrast, the present AD converter system is directed to only eliminating the DC component and input signal, to allow for higher resolution of the AC component. The DC component is separately digitized and added to the AC converted output.

15   **BRIEF SUMMARY OF THE INVENTION**

The present AD converter system concerns those signals which have a low frequency component (such as DC) superimposed upon an AC component. The magnitude of the AC component must be less than or equal to one-half the span of the converter. The majority of signal transducers, such as pressure to voltage converters,

20   satisfy this requirement. For these signals, the present invention provides a high resolution ADC with the simplicity advantage inherent in a reduced resolution ADC. This is accomplished by first connecting the input signal through a programmed gain

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preamplifier. The preamplifier matches the full range of the ADC to only the AC

component portion of the input signal. In order to cover the entire input signal, the

ADC's range is complemented by an offset value. The advantage of this technique is

the preamplifier, designed to amplify the input signal at high gain, while applying the

5   offset value at low gain. A digital summing junction combines the analog to digital

conversion results with the offset value, resulting in a higher precision overall

conversion.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

Figure 1 is an example of a system having a full-scale analog to digital converter.

10   The vertical axis is the input span of the analog to digital converter;

Figure 2 is an example of a system having a partial-span analog to digital

converter. The shaded region is the converter's span;

Figure 3 is an example of a system having a partial-scale analog to digital

converter whose spans are offset as needed to digitize the entire input signal;

15   Figure 4 is a block diagram of an analog to digital converter system according to

an embodiment of the invention;

Figure 5 is a circuit diagram of a programmable gain preamplifier having

adjustable offset in accordance with an embodiment of the invention;

Figure 6 is a block diagram of the calibration process of the AD converter

20   system in accordance with an embodiment of the invention; and

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Figure 7 is a block diagram of the present AD converter system showing waveshapes during operation of the system.

DETAILED DESCRIPTION OF THE INVENTION

Reduced Span Analog to Digital Converter

5   To attain the simplicity advantage inherent in a reduced-resolution analog to digital converter, such a device is first connected to the input signal through a programmed gain preamplifier. Figure 2 shows the result of applying an input signal through such an amplifier to the analog to digital converter.

The programmed gain preamplifier matches the span of the analog to digital

10   converter against only a portion of the system input, as illustrated by the example of Fig. 2. The analog to digital converter's span covers only system inputs ranging between -0.005 to +0.005. By way of example, this corresponds to ¼ the span of the converter described in Fig. 1. It is important to note however, that if the analog to digital converter represented in Fig. 2 has ¼ the resolution of the converter represented in Fig.

15   1, both converters can resolve the limited span between -0.005 and +0.005 to the same resolution.

Offset Steps

The entire input signal range, from -0.01 to +0.01 in the example of Fig. 2, still requires coverage, however. This requirement can be met by vertically positioning the

20   converter's span by means of an offset value. Figure 3 shows this effect.

In Fig. 3, the span of the analog to digital converter is displaced along the vertical axis to one of eight overlapping positions. These are shown in the figure as shaded bands. The width of each band represents the analog to digital converter's span.

It can be appreciated from the figure that an advantage of this technique is that

5   the preamplifier is designed to amplify the input signal at high gain while applying the offset value at low gain. The offset value thus requires a system level accuracy corresponding to the preamplifier's low gain value for offset divided by its high gain value for signals.

As will be described, a digital summing junction arrangement combines the

10   analog to digital conversion results with the offset value, resulting in a higher precision overall conversion.

Offset Overlap

The offset bands illustrated in Fig. 3 are chosen to overlap, thereby providing hysteresis: The offset, once stepped to a new value, consequently need not be stepped

15   back to its previous value should the input signal change back to a value covered by the previous band. This is necessary to accommodate signals having an oscillatory component.

Input Signal Limitations

As can be appreciated, input signals suitable for digitization by this technique are

20   limited to those consisting of a low-frequency component (such as DC) upon which is superimposed an AC component. The magnitude of the AC component must be less

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than or equal to one-half the span of the converter. The majority of signal transducers, such as pressure to voltage converters, satisfy this requirement.

Turning now to Fig. 4, the system diagram of the present invention includes the following components:

5   1.   Programmable gain preamplifier

      2.   Offset compensation digital summing junction

Other important components of the invention which are well known to practitioners of the art are:

      1.   Anti-alias filter

10   2.   Analog to digital converter

      3.   Digital to analog converter

Programmed Gain Preamplifier

The programmed gain preamplifier as shown in Fig. 5 provides a high differential gain for the input signal and a low single-ended gain for the offset signal.

15   This circuit has two differential inputs and one single-ended input. The first of the two differential inputs is for signal and the second is for calibration. The signal input is applied differentially between the terminals labeled "Non-Inverting Differential Input" and "Inverting Differential Input". Calibration uses the terminals labeled "Calibration Input" and "Inverting Differential Input". Figure 5 shows the resistor "R_{CAL}" connected

20   between the calibration inputs. Note that the terminal labeled "Inverting Differential

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Input" is used for one side of both differential inputs. The single-ended input is applied to the terminal labeled "Offset (Input) Terminal".

In the circuit of Fig. 5, the input differential gain is determined by a double-pole, eight position switch: Position 0 is the lowest gain position and position 7 is the highest

5   gain position. It should be understood that the switches in the illustrated circuit can be mechanical, as shown, or can be electronic. Either implementation is suitable.

The signal appearing on the "Output Terminal" is the electrical sum of the input (either the differential input signal or calibration, depending upon which is selected) times the amplifier's gain plus the voltage appearing on the "Offset Terminal" times a

10 gain of 1.

Offset Generation

The voltage applied to the Offset (Input) Terminal shown in Fig. 5 is provided by a digital to analog converter. In the block diagram of Fig. 4, this circuit is labeled "Digital to Analog Converter" and is shown connected to the preamplifier's offset

15 terminal.

Calibration

Calibration of the present analog to digital converter system insures accuracy. Calibration can be implemented under microprocessor control (not shown) although other means such as a digital state machine may also be used.

20   Calibration for each of the offset values shown in Fig. 3 is required. This entails first switching the programmable gain preamplifier of Fig. 5 across the calibration

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resistor. This applies the equivalent of zero volts to the preamplifier's input so that any

voltage appearing at its output is due entirely to preamplifier error voltages summed

with voltages on its offset terminal. The first value of offset is then applied to the offset

terminal. The resulting waveform is digitized by the 12-bit analog to digital converter

5   and is stored in memory.

The stored waveform is the calibration waveform for use when the offset is

switched from zero to the first value of offset. This waveform is to be *subtracted* from

the output signal whenever the offset is switched from zero to the first value of offset.

This process is repeated as the offset is switched from its first value to its second

10   value to create a second calibration waveform. The process is repeated for each of the

offset transitions between adjacent values of offset, both up and down, resulting in 14

different calibration waveforms.

The appropriate calibration waveform is to be *subtracted* on a sample-by-sample

basis whenever the offset value steps from one band to the next. The calibration

15   waveform must be applied synchronously with the offset step, in the aforementioned

digital manner, to the digital subtraction process.

Figure 6 is a block diagram of this process for the generation of one calibration

waveform. The waveforms shown are plots of voltages or numeric values vs. time.

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Example

Figure 7 is deemed helpful in showing how the invention operates on an example signal and includes corresponding waveforms. It should be appreciated that the input signal shown in the figure is but one example of many possible.

5   As shown in Fig. 7, the example analog input signal to the programmable gain preamplifier is a sine wave whose offset shifts in a negative direction after approximately one-third of the time plotted along the horizontal axis. The span of the analog to digital converter is insufficient to cover the entire vertical dimensions of the waveform.

10   An offset signal, as shown in the figure, is applied to the preamplifier to keep the signal within the span capability of the analog to digital converter. The output of the anti-aliasing filter consequently remains within the span of the converter.

The output of the analog to digital converter is processed digitally with one of the calibration waveforms as hereinbefore described to yield a higher-resolution, digital

15   version of the original waveform as shown in Fig. 7.

It can be appreciated from both Fig. 6 and Fig. 7 as hereinbefore described, that calibration waveforms accommodate the anti-alias filter's frequency response. As a step signal, such as the one arising from the application of an offset signal to the preamplifier, is applied to a low-pass anti-alias filter, the output of the filter has a finite

20   rather than instantaneous rise time. This somewhat gradual transition is subtracted out since it is a replica of the waveform originally obtained during calibration.

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